INDIAN INSTITUTE OF TECHNOLOGY MANDI

KAMAND, DISTT. MANDI – 175005 (HIMACHAL PRADESH)

MINUTES OF 32ND BOARD OF ACADEMICS MEETING

VENUE	:	A-4 CONFERENCE ROOM, KAMAND
DATE	:	05th DECEMBER, 2019 (THURSDAY)
TIME	:	04:00 P.M.

Following members attended the meeting

Sl.No	Responsibilities	Name
1	Dean Academics	Dr. Pradeep Parameswaran
2	Associate Dean (Courses)	Dr. Anil K Sao
3	Chairman Library Advisory Committee	Dr. Astrid Kiehn
4	Chairman Course Proposal Committee + Nominee (SCEE)	Dr. Kunal Ghosh
5	Course Coordinator (IC Courses)	Dr. Aniruddha Chakraborty
6	Course Coordinator (MA Dev. Studies) + Nominee (SHSS)	Dr. Shyamasree Dasgupta
7	Course Coordinator (B.Tech.-EE)	Dr. Shubhajit Roy Chowdhury
8	Course Coordinator (M.Tech.- (Energy Engg. (Materials))	Dr. Atul Dhar
9	Course Coordinator (M.Tech.-(Mechanical Engg. (Energy Systems))	
10	Course Coordinator (M.Tech.-(VLSI))	Dr. Hitesh Shrimali
11	Course Coordinator (M.Tech.-(Communication and Signal Processing))	Dr. Samar Agnihotri
12	Course Coordinator (M.Tech.-Biotechnology)	Dr. Shyam K Masakapalli
13	Course Coordinator (M.Sc.-Physics) + (I-Ph.D. (Physics))	Dr. Ajay Soni
14	Nominee-2: School of Engineering	Dr. Venkata Uday Kala
15	Nominee-2: School of Computing & Electrical Engineering	Dr. Aditya Nigam
16	Nominee-2: School of Basic Sciences	Dr. Prosenjit Mondal
17	Nominee-1: School of Humanities & Social Sciences	Dr. Suman Sigroha
18	Research Affairs Secretary	Mr. Partha S. Nayak
19	Assistant Registrar (Academics): Secretary	Mr. Vivek Tiwari

Following members could not attend the meeting

Sl.No.		Name	
1	Associate Dean (Research)	Dr. Rahul Vaish	Member
2	Course Coordinator M.Sc. (Chemistry)	Dr. Chayan K Nandi	Member
3	Course Coordinator (B.Tech.-CSE)	Dr. Dileep A D	Member
4	Course Coordinator (B.Tech.-ME)	Dr. Arpan Gupta	Member
5	Course Coordinator (B.Tech.-CE)	Dr. Deepak Swami	Member
6	Course Coordinator (M.Tech.-(Power Electronics and Drives))	Dr. Narsa Reddy Tummuru	Member
7	Course Coordinator (M.Sc.-Applied Maths)	Dr. Nitu Kumari	Member
8	Nominee-1: School of Engineering	Dr. Rajesh Ghosh	Member
9	Nominee-1: School of Basic Sciences	Dr. Syed Abbas	Member
10	Academic Affairs Secretary	Mr. Anand Ramrakhyani	Member
11	Industry Member – 1	Dr. Nadeem Akhtar	Member

Special Invitee

Sl.No.	Name	
1.	Dr. Trayambak Basak	Asst. Prof., SBS
2.	Dr. Pradeep Kumar	Asst. Prof., SE
3.	Dr. Gaurav Bhutani	Asst. Prof., SE
4.	Dr. Parmod Kumar	Asst. Prof., SE

PART-A

(Issues discussed by the Board of Academics when the Student Members were present)

32.1 Confirmation of the minutes of 31st meeting of Board of Academics:

The minutes of the 31st Board of Academics meeting held on 17th September, 2019 were confirmed with following modification.

Point No. 31.6 "*Academic Secretary briefed the Board on the proposal for flexibility in internship requirements for the B.Tech. students. BoA rejected the proposal after detailed discussion*"

REPLACED BY

"*Academic Secretary briefed the Board on the proposal for flexibility in internship requirements for the B.Tech. students. BoA rejected the proposal after detailed discussion, however the Dean (Academics) pointed that in a few cases, the students can do the internship at other time periods as mentioned in the B.Tech. Ordinance and Regulations, R.25.1.*"

32.2 To consider approval of courses presented by the Course Proposal Committee (CPC):

No course was presented for approval. Chairperson, CPC informed BoA about certain difficulties being faced in the course proposal approval. After due deliberations, the following were decided:

(i) If there is enough expertise (2 or more faculty apart from the proposer) available in an area in the institute, a new course proposal need not be sent to external evaluation. The CIG can meet physically, review the proposal and minute the decision accordingly. The revised course proposal along with the CIG minutes can be sent to CPC Chair for further processing. All other routine processes like posting on FDB etc. need to be followed in this case as well.

(ii) If there is no expertise available in an area in the institute, a new course proposal needs to be sent to external review.

32.3 To consider the proposal to offer new Minor programmes from SCEE:

Dr. Hitesh Shrimali briefed BoA the proposal to offer new Minor programs from SCEE. Considering the fact that the Free Elective basket has now been increased to 22 credits, BoA felt that the credit requirements of Minor can be increased from the existing 9 to 12-15 credits. Accordingly, Dr. Hitesh Shrimali was requested to rework the minor proposals taking inputs of faculty from Mechanical Engineering and present the proposal in a subsequent BoA.

32.4 To consider the modification in B.Tech. EE discipline course list:

Dr. Shubhajit Roy Chowdhury made a proposal to BoA for modification of B.Tech. EE discipline course list. After due deliberations, the BoA recommended the modification with minor changes for consideration by the Senate for it's approval. The final modified proposal is placed at **Annexure – A**.

32.5 To consider the IC 241 course as compulsory in Science I basket for B.Tech. Bioengineering students:

Dr. Shubhajit Roy Chowdhury briefed BoA the proposal to consider IC 241(Materials Science for Engineers) as a compulsory course in Science I basket for Bioengineering students. After due deliberations, the BoA recommended the proposal with minor modification for consideration by the Senate for it's approval. The final modified proposal is placed at **Annexure – B**.

32.6 To consider the proposal to consider some credits as Pass/Fail grade towards the requirement of degree completion:

Dr. Anil K Sao briefed BoA the proposal to consider some credits as Pass/Fail grade towards the requirements of degree completion. After due deliberations, the BoA recommended the proposal with minor modification for consideration by the Senate for it's approval. The final modified proposal is placed at **Annexure – C**.

32.7 To consider modification in M.Tech. in Mechanical Engineering with Specialization in Energy Systems programme starting from August 2020:

Dr. Pradeep Kumar briefed BoA the proposal to consider modification in M.Tech. in Mechanical Engineering with Specialization in Energy Systems programme. BoA noted that in effect, this is a new M.Tech. programme proposal. Therefore, Dr. Pradeep Kumar was requested to follow the general approval process which includes brainstorming meeting with external academic and industry experts and present the modified proposal for approval of BoA in a subsequent meeting.

32.8 Any other item with the permission of the Chair.

In addition to the circulated agenda points, with the permission of Chairman, BoA considered the following items:

(a) Dr. Suman Sigroha, briefed the BoA certain points regarding SHSS course baskets for B.Tech. The board deliberated and suggested some minor changes. She was requested to modify the proposal accordingly. As the changes are minor, BoA recommended to take approval of Chairman, Senate and report the same to Senate accordingly.

(b) Dr. Samar briefed BoA that a Ph.D. student's registration is cancelled if s(he) is unable to clear the comprehensive exams in two attempts as per regulation R.18. Allowing such a student to immediately apply for the Ph.D. program in the institute will be a mockery of the entire process of evaluation, because in such scenarios a student who has failed to fulfill even the minimum requirements of a Ph.D.

program as set by the institute will be allowed for admission to the same program. The board discussed and recommended for Senate's approval that MS/Ph.D. regulations be amended to take care of such scenarios and proposed a cooling off period of minimum three years for students who failed to clear comprehensive examination before consideration for admission to any program of IIT Mandi.

The meeting ended with a vote of thanks to the Chair.

Secretary, Board of Academics

16/1/2020

Chairman, Board of Academics

Annexure A

Recommendation

EE Discipline Core Courses and Sequencing

w.r.t.: IC CIG meeting held on July 17th, 2019 and School meeting held on July 23, 2019

As per the IC CIG meeting held on July 17th, 2019:

"

1) Three baskets were made (courses of 24 credits) namely: Science I, Science II and Engineering Science
2) A student must take one course from each basket. Here, CIG can make a course compulsory for specific discipline. This should be done by 26th July 2019.
3) Engineering thermodynamics course will be offered as 3 credit course.
4) 12 credits will be used as 3 (Discipline core) + 9 (Free Elective)

Course coordinator should take appropriate action to implement this recommendation from Aug 2019.

"

In School meeting held on July 23, 2019, IC CIG outcome as mentioned above was discussed and following modifications was agreed to be included in EE Discipline Core :

1) EE 208P (1-0-2-2) Digital Systems Design Practicum will be modified to EE 210 Digital Systems Design (3-0-0-3) and EE 210P Digital Systems Design Practicum (0-0-2-1)
2) EE 312P Microelectronics Circuits Design (MCD) Practicum will be removed.
3) EE 211 (2-0-2-3) Analog Circuit Design and EE 211P (0-0-2-1) Analog Circuit Design Lab will be introduced.
4) IC260 Signals and Systems from IC Engineering Science basket will be compulsory for EE UG students as this course forms the prerequisite for other UG EE DC courses.
5) IC XXX Measurement and Instrumentation Practicum from IC Engineering Science basket will be compulsory for EE UG students from Discipline Elective or Free Elective basket and it will serves as a prerequisite for the award of the B.Tech (EE) degree.
6) If approved by Senate, above mentioned changes should be made effective for intake batch of 2018 and onwards.
7) Table I shows the changes in the Discipline core courses.

Previous DC courses	Credit Structure	Semester	Current DC courses	Credit Structure	Semester
Digital System Design Practicum (EE208P)	1-0-2-2	4th Semester	Digital System Design (EE210 & EE210P)	3-0-0-3 (EE210) and 0-0-2-1(EE210P)	3rd Semester
Network Theory (EE203)	2.5-0.5-0-3	4th Semester	Network Theory (EE203)	2.5-0.5-0-3	4th Semester
Electromechanics (EE201 and EE201P)	2.5-0.5-0-3 (EE201) 0-0-2-1(EE201P)	4th Semester	Electromechanics (EE210 and EE210P)	2.5-0.5-0-3 (EE201) 0-0-2-1(EE210P)	4th Semester
Computer Organization (CS201 and CS201P)	3-0-0-3 (CS201) 0-0-2-1(CS210P)	5th Semester	Computer Organization (CS201 and CS201P)	3-0-0-3 (CS201) 0-0-2-1(CS210P)	5th Semester
Control Systems (EE301 and EE301P)	3-0-0-3 (EE301) 0-0-2-1(EE301P)	6th Semester	Control Systems (EE301 and EE301P)	3-0-0-3 (EE301) 0-0-2-1(EE301P)	5th Semester
Power Systems (EE303)	3-1-0-4	6th Semester	Power Systems (EE303)	3-1-0-4 (EE303)	5th Semester
Communication Theory (EE304 and EE304P)	3-0-0-3 (EE304) 0-0-2-1(EE304P)	6th Semester	Communication Theory (EE304 and EE304P)	3-0-0-3 (EE304) 0-0-2-1(EE304P)	4th Semester
Device Electronics for Integrated Circuits (EE311)	3-0-0-3	5th Semester	Device Electronics for Integrated Circuits (EE311)	3-0-0-3	3rd Semester
Microelectronics Circuit Design Practicum (EE312P)	0-0-3-2	5th Semester	Analog Circuit Design (EE211 and EE211P)	2-0-2-3 (EE211) 0-0-2-1(EE211P)	4th Semester

Following Committee was constituted to propose suggestive sequencing of EE DC courses and to form the syllabus for EE 208 Digital Systems Design (3-0-2-4) and EE 2XX (3-0-0-3) Analog Electronics

Dr. Rahul, Chair

Dr. Shubhajit

Dr. Arnav

Dr. Hitesh

Dr. Narsa

Dr. Kunal

Committee propose following suggestive sequencing of EE DC courses and syllabii of EE 210&P Digital Systems Design (3-0-2-4) and EE 211&P (2-0-4-4) Analog Circuit Design as given in subsequent pages. However, it is important to note that Students are free to decide to follow any sequencing of discipline core courses as per their requirements subject to full-fillment of pre-requisite requirements.

Suggestive Sequencing of EE DC courses

EE 210&P Digital System Design (3rd semester)

EE 203 Network Theory (3rd semester)

EE 311 Device Electronics for Integrated Circuits (3rd semester)

EE 201&P Electromechanics (4th semester)

EE 211&P Analog Circuit Design (4th semester)

EE 304&P Communication Theory (4th semester)

CS 201&P Computer Organization (5th semester)

EE 301&P Control Systems (5th semester)

EE 303 Power Systems (5th semester)

Corresponding placement of EE DC courses Semester wise is as follows:

Semester I

Course Code	L-T-P-C	Course Name
IC110	2.5-0.5-0-3	Engineering Mathematics
IC152	3-0-3-4	Data Science I
IC160	3-0-0-3	Electrical Systems Around Us
IC160P	0-0-3-2	Electrical Systems Around Us Lab
IC140	2-0-3-4	Graphics for Design
IC101P	0-0-3-2	Reverse Engineering
HS106	3-0-0-3	English I
HS10X	1-0-0-1	Creative Understanding
Total	**22 credits**	

Semester II

Course Code	L-T-P-C	Course Name
IC111	2.5-0.5-0-3	Linear Algebra
IC141	2-0-0-2	Product Realization Technology
IC141P	0-0-3-2	Product Realization Technology Lab
IC161	3-0-0-3	Applied Electronics
IC161P	0-0-3-2	Applied Electronics Lab
IC252	3-0-2-4	Data Science II
IC142	3-0-0-3	Engineering Thermodynamics
HSXX1	3-0-0-3	HSS Language competence basket course
Total	**22 credits**	

Semester III

Course Code	L-T-P-C	Course Name
IC260 (IC basket course)	2.5-0.5-0-3	Signals and Systems (Compulsory for EE student from Engg. Science basket)
IC240	3-0-0-3	Mechanics of Rigid Bodies
IC2XX	2-0-2-3	Data Science III
EE208	3-0-2-4	Digital Systems Design
EE203	2.5-0.5-0-3	Network Theory
EE311	3-0-0-3	Device Electronics for Integrated Circuits
HSXX2	3-0-0-3	HSS basket course
Total	**22 credits**	

Semester IV

Course Code	L-T-P-C	Course Name
IC201P	0-0-6-4	Design Practicum
ICXXX (IC basket course) or IC M&I Practicum as Free Elective	3-0-0-3	Science-I IC basket course or M&I Practicum
EE2XX	2-0-2-3	Analog Circuit Design
EE201+EE201P	2.5-0.5-2-4	Electromechanics
EE304 + EE 304P	3-0-2-4	Communication Theory
EEXX1	3-0-0-3	Discipline Elective-I
Total	**21 credits**	

Semester V

Course Code	L-T-P-C	Course Name
ICXXX or IC M&I Practicum as Free Elective	3-0-0-3	Science-II IC basket course or M&I Practicum
IC221	3-0-0-3	Foundations of Electrodynamics
CS201+CS201P	3-0-2-4	Computer Organization

EE301 + EE 301P	3-0-2-4	Control Systems
EE303	3-1-0-4	Power Systems
EEXX2	3-0-0-3	Discipline Elective-II
Total	**21 credits**	

Semester VI

Course Code	L-T-P-C	Course Name
IC222P	0-0-3-2	Physics Practicum
EEXX3	3-0-0-3	Discipline Elective-III
EEXX4	3-0-0-3	Discipline Elective-IV
FEXX1	3-0-0-3	Free Elective-I
FEXX2	3-0-0-3	Free Elective-II
HSXX3	3-0-0-3	HSS basket course
DP301P/EEXX5	0-0-6-4	Interdisciplinary Socio Technical Practicum/ Discipline Elective-V
Total	**21 credits**	

Semester VII

Course Code	L-T-P-C	Course Name
ITXX1	0-0-2-2	Industrial Internship
FEXX3	3-0-0-3	Free Elective-III
FEXX4	4-0-0-4	Free Elective-IV
HSXX1	3-0-0-3	HSS Elective-I
DP401P/EEXX6	0-0-6-3	Major Technical Project-I/Discipline Elective-VI
Total	**15 credits**	

Semester VIII

Course Code	L-T-P-C	Course Name
FEXX5	3-0-0-3	Free Elective-V
FEXX6	3-0-0-3	Free Elective-VI
FEXX7	3-0-0-3	Free Elective-VII
HSXX2	2-0-0-2	HSS Elective-II
DP402P/EEXX7	0-0-10-5	Major Technical Project-I/Discipline Elective-VII
Total	**16 credits**	

New Course Proposal

Course number: EE211

Course name: Analog Circuit Design

Credit: 2-0-2-3 (L-T-P-C)

Prerequisite: Network theory (EE203), Applied Electronics (IC161)

Intended for: BTech (EE)

Elective or Core: Core for B. Tech. (EE) and Elective for other UG Programmes

Semester: Even/Odd

Preamble and Objectives: Analog Circuit Design course is designed to build a strong foundation in both design and analysis of electronic circuits by mixture of lectures and having relevant experiments. This course syllabus offers conceptual understanding and mastery of the material by using modern examples to motivate and prepare IIT Mandi's undergraduate students for advanced courses and their careers. The course has unique problem-solving framework enables the students to deconstruct complex active circuits into small signal equivalent model that they are familiar with which builds the confidence and intuitive skills needed for success. To succeed in the practice of electronics in industry, students must develop the ability to think intuitively about circuits. They need to move beyond simply plugging and chugging numbers in equations and be prepared to face real design trade-offs. The course components also help students to develop intuitive techniques so they can design and implement circuits not just analyse them. Using many real-word examples and applications will motivate the student to understand the importance of today's microelectronics. Some of the most common electronics applications of analog circuit designing viz. power amplifiers, oscillators, wave shaping circuits, PLL, ADCs and DACs have been kept at the end of this course. The course is intended for advance stream of studies such as communication engineering, power electronics and very large scale integration (VLSI).

Course modules:

Lecture modules:

- **BJT/MOS single stage amplifiers, cascade and cascodes [6 hrs]**

  - Large signal and small-signal model, biasing, input and output impedance, operating point calculations and design, single ended BJT/CMOS amplifiers, cascade and cascode amplifiers

- **BJT/MOS Current mirrors [3 hrs]**

- PVT independent normal current mirror, cascode current mirror, regulated current mirror and Wilson current mirror

- **Differential Amplifiers** **[3 hrs]**

- MOS/BJT Differential Pair, qualitative large/small signal analyses, differential pairs with active loads and common-mode rejection

- **BJT/MOS Frequency Response** **[3 hrs]**

- High frequency model of single ended and differential amplifiers, Frequency response: magnitude and phase plot calculations

- **Feedback theory** **[3 hrs]**

- Properties of negative and positive feedback, loop gain calculations, types of amplifiers, voltage controlled current source (VCCS), current controlled current source (CCCS), current controlled voltage source (CCVS), voltage current voltage source (VCVS), stability analyses under negative feedback topology.

- **Output stages and power amplifiers** **[3 hrs]**

- Emitter follower as power amplifier, push-pull amplifier, cross-over distortions, large signal considerations, heat dissipation, efficiency, Classes of amplifiers

- **Oscillators and phase locked loop** **[4 hrs]**

- Barkhausen criteria of oscillation, bistable, monostable and astable multi vibrators, LC, relaxation, phase shift and Colpit oscillators, phase locked loop concept and its understanding, signal generation and wave shaping circuits.

- **Data converters** **[3 hrs]**

- Digital-to-analog converters (DAC): R-2R, current scaling and voltage scaling

- Analog-to-digital converter (ADC): flash, SAR, single slope, dual slope, pipeline and sigma-delta modulator

Course number: EE211P

Course name: Analog Circuit Design Lab

Credit: 0-0-2-1 (L-T-P-C)

Prerequisite: Network theory (EE203), Applied Electronics (IC161)

Intended for: BTech (EE)

Elective or Core: Core for B. Tech. (EE) and Elective for other UG Programmes

Semester: Even/Odd

Experiment modules:

1. Lissajous pattern generation and its understanding.
2. Understanding of net-listing using SPICE simulations.
3. Understanding of I-V characteristics of BJT/MOS transistor.
4. Common emitter amplifier design.
5. Understanding of MOS class-AB pull-pull amplifier using CD4007 IC.
6. Active filter design using operational amplifier.
7. Operation of PLL understanding using 565 IC.
8. Operation of SAR understanding using 0808/0809 IC.
9. Project on analog circuit application.

Text book:

1. "Fundamentals of microelectronics" by Behzad Razavi, Wiley, Apr., 2013.

Reference book:

1. "Microelectronic Circuits-Theory & Applications" by A.S. Sedra and K.C. Smith, 7th Edition, Oxford University Press, Jun. 2017.

Other Faculty interested in teaching this course:

Proposed by: Dr. Hitesh Shrimali, Dr. Rahul Shrestha, Dr. G. Shrikanth Reddy

School: SCEE

Signature: Dr. Hitesh Shrimali Date: Aug. 1, 2019

Recommended/Not Recommended, with Comments:

_____ Date:_____

Chairman, CPC

Approved / Not Approved

_____ Date:_____

Chairman, Senate

Digital System Design

Course Number: EE-210
Credits: L-T-P-C: 3-0-0-3
Course Name: Digital Systems Design.
Students Intended: B. Tech (EE).
Semester: Even/Odd.
Elective or Core: Core for B. Tech (EE) & Elective for other UG programs.
Pre-requisite: Applied Electronics (IC161) and Applied Electronics Lab (IC161P).

Preamble & Objective:

A primary objective of this course is to create strong foundation of digital design in our students. This course inculcates deeper understanding of the subject in students that will enable them to design and understand various real-world digital systems. Any subject becomes interesting to student when they gather hierarchical understanding of the topics in detail fashion and then escalate to next-level by applying this knowledge to develop their own system to cater the real-world problems. The content of this course renders exactly the same experience to the students.

Course Content:

1. **Combinational Logic Design with MSI Components and Programmable Logic Devices**: 1.1 Binary Adders and Subtractors {*Cascading Full-Adders, Carry Look-ahead Adder, High-speed Adders using Carry Look-ahead Principles, using MSI Adders as Subtractors, BCD Adder, using MSI adder as code converter*}; 1.2 Arithmetic Logic Unit; 1.3 Binary Multipliers; 1.4 Array Multipliers; 1.5 Tristate Buffers; 1.6 Combinational Logic Hazards {*Static and Dynamic Hazards*}. [4 hours]

2. **Flip-Flops and Simple Flip-Flop Applications**: 2.1 Basic Bi-stable Element; 2.2 Application of the SR Latch as Switch De-bouncer; 2.3 Gated SR and D Latch; 2.4 Timing Considerations
{*Propagation Delays, Contamination Delays, Minimum Pulse Width, Setup and Hold Times*}; 2.5 Pulse Triggered Master-Slave Flip –Flops {*SR & JK Master-Slave Flip-Flops, 0's and 1's Catching*}; 2.6 Edge Triggered Flip-Flops {*Positive & Negative Edge Triggered Flip-Flops, Master Slave Flip-flops with Data Lockout*}; 2.7 Characteristics Equations; 2.8 Registers; 2.9 Counters; 2.10 Design of Synchronous Counters; 2.11 Self-Correcting Counters. [5 hours]

3. **Synchronous Sequential Networks and Algorithmic State Machine (ASM)**: 3.1 Introductions to State Equivalence; 3.2 State Reductions {*Equivalence Classes and Implication Charts*}; 3.3 State Reduction of Incompletely Specified State Table using Merger Graphs; 3.4 State Assignment Techniques {*State Assignment Permutations, State Assignment Algorithm, Implication Graph*}; 3.5 Algorithm State Machine {*ASM Symbols, Elapse Time Measurement as an ASM Design Example*}; 3.6 Linked Sequential Machines. [3 hours]

4. **Asynchronous Sequential Networks**: 4.1 Fundamental and Pulse Mode Asynchronous Sequential Machines; 4.2 Analysis of Asynchronous Sequential Machines; 4.3 Deriving Flow Table; 4.4 State Assignment; 4.5 Asynchronous Design Problems; 4.6 Data Synchronizers; 4.7 Mixed Operating Mode Asynchronous Circuits. [7 hours]

5. **Programmable Logic and Memory**: 5.1 Introductions to Memory {*ROM, PROM and EPROM*}; 5.2 Using and EPROM to Realize a Sequential Circuit; 5.3 Programmable Logic Devices {*PLA, PAL, GAL*}; 5.4 Erasable Programmable Logic Devices; 5.5 PLD Computer-Aided Design {*PLD Realization of Combinational Logic, Realization of truth table, flip-flops and state machine using PLD language*}. [5 hours]

6. **Hardware Description Language and Field-Programmable Gate-Array (FPGA)**: 6.1 Introductions to Hardware Description Language (HDL); 6.2 Overview of Structural, Behavioral and Dataflow Modeling of Digital Systems using HDL; 6.3 HDL Realizations of Finite State Machines, Delay Modeling, Memory Modeling; 6.4 Synthesizable & Non-Synthesizable HDL Codes for Digital System Design; 6.5 Overview of FPGA architecture; 6.6 Realization of Data-Path and Controller; 6.7 Timing Analysis of Data-Path and Controller; 6.8 Synthesis, Placement, Routing and Performance Optimization; 6.9 Implementation of Simple Digital Systems using FPGA Exercising the Timing Closure Paths. [7 hours]

7. **Microcontroller and Real-World Applications**: 7.1 Introduction to microcontrollers; 7.2 Architectural Overview of a Typical Microcontroller such as AVR Microcontroller; 7.3 Addressing; 7.4 Assembly Language Programming; 7.5 Interfacing with I/O devices, timer/counter programming, interrupt processing etc; 7.6 Interfacing with Simple Devices such as LCD, Keyboard, Motor Control, Sensors, LED 7 Segment Display, DTMF decoder etc; 7.7 SPI, I^2C, Programmable Interrupt Controller, USART etc. [9 hours]

Course Number: EE-210P
Credits: L-T-P-C: 0-0-2-1
Course Name: Digital Systems Design Practicum

Experimental Modules for EE-210P:

- Basics understanding of hardware descriptive language (Verilog / VHDL / System Verilog). Netlist synthesis, functional (Behavioral) & post-route simulations, and hardware prototyping on FPGA using latest design suites (like Xilinx ISE or Vivado or Model Sim etc.).

  [2 hours]
- Design and implementation of basic gates, multiplexers, de-multiplexers, various adders and multipliers in FPGA platform.

  [1 hours]
- FPGA implementations of flip-flops, registers, counters and circuitry verifying the register delays.

  [1 hours]
- Design and implementation of Processor ALU on FPGA.

  [2 hours]
- Design and implementations of random access memory (RAM) and read only memory (ROM). These experiments must include the reading and writing operations of RAM for various applications.

  [1 hours]
- Understanding the static timing analysis of simple sequential circuits. It must demonstrate the two major states of any sequential circuits: timing violated and timing met states.

  [2 hours]
- Embedded experiments on LED and 7-segment displays.

  [1 hours]
- Embedded experiment on Interfacing the LCD and LDR.

  [2 hours]
- Embedded experiments on interfacing servo motor with ultrasonic.

  [2 hours]

Text books:

1. Donald D. Givone, "Digital Principles and Design", Tata McGraw-Hill Edition (2012).
2. John M. Yarbrough, "Digital Logic (Applications and Design)", Cengage Learning (2011).

Reference books:

1. Dhananjay Gadre, "Programming and Customizing the AVR microcontroller", Tata McGraw Hill, 2014.
2. Wayne Wolf, "FPGA based Systems Design", Pearson Education, 2003.
3. Stephen Brown and Zvonko Vranesic, "Fundamentals of Digital with VHDL Design", McGraw Hill, 2008.
4. Volnei A. Pedroni, "Circuit Design with VHDL", The MIT Press, 2004.
5. Steve Kilts, "Advanced FPGA Design: Architecture, Implementation and Optimization", J.Wiley and Sons, 2007.
6. Seetharaman Ramachandran, "Digital VLSI Systems Design", Springer Verlag, 2012.

7. Peter J. Ashenden, "The designer's guide top VHDL", Morgan Kaufmann, 2008.
8. Charles H. Roth Jr., "Digital Systems Design using VHDL", Cengage Learning, 2014.

Approvals:

Other Faculty interested in teaching this course: Dr. Rahul Shrestha, Dr. Shubhajit Roy Chowdhury, Dr. Hitesh Shrimali, and Dr. Srinavasu Bodapati.

Proposed by: Dr. Rahul Shrestha, Dr. Shubhajit Roy Chowdhury, and Dr. Hitesh Shrimali.

School: School of Computing & Electrical Engineering.

Signature: Dr. Rahul Shrestha Date: 1st of August, 2019

Recommended/Not Recommended, with Comments:

_____ Date: _____
Chairman, CPC

Approved/Not Approved

_____ Date: _____
Chairman, Senate

Program Structur B.Tech in Electrical Engineering

Semester	Course 1	Course 2	Course 3	Course 4	Course 5	Course 6	Course 7	Course 8	Course 9	Credits
1	IC 110	IC 140	IC 152	IC 160	IC 160P	IC 101P	HS10X	HS106		
	Engineering Mathematics	Graphics for Design	Data Science 1	Electrical Systems Around Us	Electrical Systems Around Us Lab	Reverse Engineering	HSS Core (Creative Understanding)	English I or students needing support in Englis		
	3	4	4	3	2	2	1	3		19(nwE)/22(wE)
2	IC 111	IC 142	IC 252	IC 161	IC 161P	IC 141	IC 141P	HSS		
	Linear Algebra	Engineering Thermodynamics	Data Science 2	Applied Electronics	Applied Electronics Lab	Product Realization Technology	Product Realization Technology Lab	English II or German I		
	3	3	4	3	2	2	2	students not needing support in English)		22(nWE)/19(wE)
3	EE 210	EE 203	EE 311	IC2XX	IC260	IC240	HSXXX			
	Digital Systems Design	Network Theory	Device Electronics for Integrated Circuits	Data Science 3	Signals and Systems (Engineering Sciences basket)	Mechanics of Rigid bodies	HSS Core (Communication Skills basket)			
	4	3	3	3	3	3	3			22
4	IC 201P	ICXXX	EE2XX	EE201	EE304	EEXX1				
	Design Practicum(DP)	Science I basket or MI Practicum	Analog Circuit Design	Electromechanics	Communication Theory	Discipline Elective I				
	4	3	3	4	4	3				21
5	ICXXX	CS201	EE301	EE303	EEXXX	HSXXX				
	Science II basket	Computer Organization	Control Systems	Power Systems	Discipline Elective II	HSS Core (Social Competence)				
	3	4	4	4	3	3				21
INTERNSHIP(Ungraded)										2
6	IC221	IC222P	EEXXX	EEXXX	YYXXX	DP301P				
	Foundations of Electrodynamics	Physics Practicum	Discipline Elective III	Discipline Elective IV	Free Elective I	ISTP				
	3	3	3	3	3	4				19
7	YYXXX	YYXXX	YYXXX	HSXXX	HSXXX	DP401P_EE				
	Free Elective II	Free Elective III	Free Elective IV	HSS Core (Managerial Competence)	HSS Elective	Major Technical Project				
	3	3	3	3	3	3				18
8	DP 402P_ME	YYXXX	YYXXX	YYXXX	HSXXX					
	Major Technical Project	Free Elective V	Free Elective VI	Free Elective VII	HSS Elective					
	5	3	3	4	3					18
									Total	**162**

wE=Needing support in
Not needing support in E

Order of IC Basket, HSS, DE can be changed

Program Structure		B.Tech M.Tech Integrated Dual Degree in Bioengineering									
Semester	**Course 1**	**Course 2**	**Course 3**	**Course 4**	**Course 5**	**Course 6**	**Course 7**	**Course 8**	**Course 9**	**Credits**	
1	IC 110	IC 140	IC 152	IC 160	IC 160P	IC 101P	HS10X	HS106			
	Engineering Mathematics	Graphics for Design	Data Science 1	Electrical Systems Around Us	Electrical Systems Around Us Lab	Reverse Engineering	HSS Core (Creative Understanding)	English I (For students weak in English)			
	3	4	4	3	2	2	1	3		19(nwE)/22(wE)	wE=Weak in English
2	IC 111	IC 142	IC 252	IC 161	IC 161P	IC 141	IC 141P	HSS			nwE=Not weak in English
	Linear Algebra	Engineering Thermodynamics	Data Science 2	Applied Electronics	Applied Electronics Lab	Product Realization Technology	Product Realization Technology Lab	English II or German I			
	3	3	4	3	2	2	2	3		22(nWE)/19(wE)	
3	BEXX1	BEXX2	IC136	IC2XX	IC260	IC240	HSXXX				
	Biology-I	Biology-II	Understanding Biotechnology and its applications (Science-II basket)	Data Science 3	Signals and Systems (Engineering Sciences basket)	Mechanics of Rigid bodies	HSS Core (Communication Skills basket)				
	4	3	3	3	3	3	3			22	
4	IC 201P	IC241	BEXX3	BEXX4	BEXX5	BEXX6					
	Design Practicum(DP)	Material Science for Engineers (Science I basket)	Biology-III	Physics and Modeling of Biological Systems	Computational Biology	Biostatistics					

	4	3	3	4	3	4				21	
5	BEXX7	BEXX8	BEXX9	BEXX10	BEMC1	BEMC2	BEMC2				
	Biomechanics	Bioethics and Regulatory Affairs	Biomaterials	Biosensing and Bioinstrumentation	M.Tech Core-I	M.Tech Core-II	HSS Core (Social Competence)				
	4	0	4	4	3	3	3			21	
INTERNSHIP(Ungraded)										2	
6	IC221	IC222P	BEMC3	BEXE1	BEXE2	BEXE3	YYXX1				
	Foundations of Electrodynamics	Physics Practicum	M.Tech Core-III	Discipline Elective I	Discipline Elective II	Discipline Elective III	Free Elective-I or ISTP				
	3	3	3	3	3	3	4			22	
7	YYXX2	YYXX3	YYXX4	HSXXX	HSXE1	BEXE4	BEXE5	HS541			
	Free Elective II or M.T.P.-I	Free Elective III	Free Elective IV	HSS Core (Managerial Competence)	HSS Elective-I	Discipline Elective IV	Discipline Elective V	Technical Communication			
	3	3	3	3	3	3	3	1		22	
8	YYXX5	YYXX6	HSXE2	BEXE6	BEXE7	BEXE8					
	Free Elective V or M.T.P.-II	Free Elective VI	HSS Elective-II	Discipline Elective-VI	Discipline Elective-VII	Mini project, Term paper and Seminar					
	5	4	2	3	3	4				21	
9	PGP-I									17	
10	PGP-II									17	

Proposal to consider credits as pass/fail course towards the degree requirement of students

Preamble:

An essential and unique aspect of the curricula at IIT Mandi for both undergraduate and post-graduate degree programs is the practicum based learning approach. Several practicum based courses have been designed to achieve the objective. Enhancing on this innovative approach, there requires a provision of courses that facilitate a student to learn and/or practice a special topic of interest but with minimal involvement of faculty. A few representative examples of such courses are independent study courses, research based academic or industrial projects and courses offered by on-line platforms like SWAYAM, NPTEL, etc. These modes of learning are used by some of the students at IIT Mandi, but they do not get any course credits for the same.

A continuing discussion is about the methodology that needs to be adopted for awarding credits to the students for such courses. Considering the divergence and multiple avenues through which these courses can be completed, doing relative grading will be difficult. An alternative is to award a commensurate credit with a Pass/Fail (P/F) grade. Thus, the committee proposes the following

1. **Maximum permissible P/F credits under this category:**

S.No	Program	No of credits
1	UG	9
2	Dual Degree	12
3	M.Sc./M.Tech/M.A	3
4	MS/PhD	3
5	I.PhD	6

Earned credits can be distributed as

B.Tech without honors: DE=3, FE=6
B.Tech with honors: DE= 6, FE=3
Dual Degree : DE=6, FE=6
M.A/M.Sc/M.Tech 3 credits can go to DE/ODE/FE

Here, DE denotes Discipline Elective and FE denotes Free Elective, ODE: Outside Discipline Elective

2. Courses that can be considered under P/F credits
   - Courses offered through Govt. approved online schemes such as NPTEL etc. It will be considered as per the guidelines already approved by Senate.
   - Self study/ Independent study course
   - Research based project work done with an instructor at IIT Mandi or at Industry.
   - Any courses (other than core courses) offered at IIT Mandi. Here student has to declare at the beginning of semester whether the given course(s) will be credited as P/F category or not to the Course Instructor as well as Faculty Advisor. Here, if marks obtained by the student is more then the cut-off of E grade, then he/she will be awarded P grade. Course Instructor will upload the grade as P in such cases.
3. In a given semester, a student should not take more then 6 credits in P/F category.
4. The registered credits under this category will be counted towards the total number of credits that can be registered by a student in a given semester.

Dr. Gaurav Bhutani

Dr. Kunal Ghosh

Dr. Anil Kumar Sao