INDIAN INSTITUTE OF TECHNOLOGY MANDI

KAMAND, DISTT. MANDI – 175005 (HIMACHAL PRADESH)

MINUTES OF 21ST BOARD OF ACADEMICS MEETING

VENUE	:	A-4 CONFERENCE ROOM, KAMAND
DATE	:	14TH DECEMBER, 2017 (THURSDAY)
TIME	:	03:00 P.M.

Following members attended the meeting

<table>
<tr><th>Sl.No.</th><th></th><th>Name</th><th></th></tr>
<tr><td>1.</td><td>Dean Academics</td><td>Prof. B.D. Chaudhary</td><td>Chairman</td></tr>
<tr><td>2.</td><td>Associate Dean (Research) i/c</td><td>Dr. Pradeep Parameswaran</td><td>Member</td></tr>
<tr><td>3.</td><td>Associate Dean (Courses)</td><td>Dr. Pradeep Parameswaran</td><td>Member</td></tr>
<tr><td>4.</td><td>Course Coordinator (SHSS Courses) + Nominee (SHSS)</td><td>Dr. Shyamasree Dasgupta</td><td>Member</td></tr>
<tr><td>5.</td><td>Course Coordinator (B.Tech.-ME)</td><td>Dr. Arpan Gupta</td><td>Member</td></tr>
<tr><td>6.</td><td>Course Coordinator (B.Tech.-CE)</td><td>Dr. Deepak Swami</td><td>Member</td></tr>
<tr><td>7.</td><td>Course Coordinator (M.Tech.- (Energy Engg. (Materials))</td><td rowspan="2">Dr. Atul Dhar</td><td>Member</td></tr>
<tr><td>8.</td><td>Course Coordinator (M.Tech.-(Mechanical Engg. (Energy Systems))</td><td>Member</td></tr>
<tr><td>9.</td><td>Course Coordinator (M.Tech.-Biotechnology)</td><td>Dr. Shyam K Masakpalli</td><td>Member</td></tr>
<tr><td>10.</td><td>Course Coordinator (M.Sc.-Applied Maths)</td><td>Dr. Nitu Kumari</td><td>Member</td></tr>
<tr><td>11.</td><td>Nominee-1: School of Engineering</td><td>Dr. Rajesh Ghosh</td><td>Member</td></tr>
<tr><td>12.</td><td>Nominee-2: School of Computing & Electrical Engineering</td><td>Dr. Aditya Nigam</td><td>Member</td></tr>
<tr><td>13.</td><td>Research Affairs Secretary</td><td>Ms. Manushree</td><td>Member</td></tr>
<tr><td>14.</td><td>Assistant Registrar (Academics): Secretary</td><td>Mr. Suresh Rohilla</td><td>Secretary</td></tr>
</table>

Following members could not attend the meeting

1.	Chairman Library Advisory Committee	Dr. Astrid Kiehn	Member
2.	Chairman Course Proposal Committee + Course Coordinator M.Sc. (Chemistry)	Dr. Chayan K Nandi	Member
3.	Course Coordinator (IC Courses)	Dr. Aniruddha Chakraborty	Member
4.	Course Coordinator (B.Tech.-CSE	Dr. Dileep A D	Member
5.	Course Coordinator (B.Tech.-EE)	Dr. Subashish Datta	Member
6.	Course Coordinator (M.Tech.-(VLSI))	Dr. Satinder Sharma	Member
7.	Course Coordinator (M.Tech.-(Communication and Signal Processing)	Dr. Renu M Rameshan	Member
8.	Course Coordinator (M.Tech.-(Power Electronics and Drives))	Dr. Narsa Reddy Tummuru	Member
9.	Course Coordinator (M.Sc.-Physics)	Dr. Chander Shekhar Yadav	Member
10.	Course Coordinator (I-Ph.D.(Physics))	Dr. Hari Varma	Member
11.	Nominee-2: School of Engineering	Dr. Venkata Uday Kala	Member
12.	Nominee-1: School of Computing & Electrical Engineering	Dr. Kunal Ghosh	Member
13.	Nominee-1: School of Basic Sciences	Dr. Syed Abbas	Member
14.	Nominee-2: School of Basic Sciences	Dr. Prosenjit Mondal	Member
15.	Nominee-1: School of Humanities & Social Sciences	Dr. Ashok Kumar	Member
16.	Academic Affairs Secretary	Mr. J Raghunath	Member
17.	Industry Member - 1	Dr. NadeemAkhtar	Member

Special Invitees attended the meeting

1.	Dr. Mahesh Reddy G.	Asst. Prof., SE
2.	Dr. Srikant Srinivasan	Asst. Prof., SCEE

PART-A

(Issues discussed by the Board of Academics when the Student Members were present)

21.1 To deliberate on change of courses curriculum in M. Tech. in EE with specialization in VLSI.

Board of Academics considered the proposal presented for changes of course curriculum for M.Tech. in EE with specialization in VLSI. In the present structure, Electrical Engineering core has 12 Credits and contains the following 04 Courses:

(i) EE 520: Microelectronic devices and modeling (3 Credits)
(ii) EE 620: Advance Digital Signal Processing (3 Credits)
(iii) CS 507 : Advance Computer Architectures (3 Credits)
(iv) ME 504: Numerical Methods for engineering Computation (3 Credits)

It is proposed to shift CS-507 (Advance Computer Architectures) with 3 credits from EE Core to VLSI specialization Elective. In place of this, EE 529 (Embedded Systems) with 4 Credits is brought from VLSI specialization elective to be part of EE Core. This change is made to strengthen the VLSI component which is based on 'Risk Architecture'. This will modify the credit for EE Core to 12-13 instead of 12.

After the recommended changes, VLSI specialization Electives will have Credits changed from 13 to 12-13, based on the choice of course below:

(i) EE 619: Mixed Signal VLSI Design (4 Credits)
(ii) EE 516: Biomedical Systems (4 Credits)
(iii) CS 507 : Advance Computer Architectures (3 Credits)
(iv) EE 510: Mathematical Methods for Signal Processing (4 Credits)

The BoA decided to recommend the proposal for Senate approval. The modified course proposal is placed at Annexure-"A":

21.2 To consider proposal for M. Tech. in Structural Engineering

The Board of Academics suggested that the proposal should be resubmitted with following details:

(i) A comparative study of similar course offered at other IITs.
(ii) Inputs received from Industry and other experts.
(iii) Expected faculty load if this course is launched.
(iv) Lab equipments and spare requirements and estimated financial liabilities need to be projected.

(v) A separate list of courses under Mathematics Core and consequent change in the 1st Semester Courses.

The Courses which are not approved by the Senate and are proposed as the part of this programme should be processed through CIG and CPC.

21.3 To revisit process and guidelines followed for effective working of Doctoral Committees.

BoA deferred deliberation on the guidelines to be presented by AD (Research).

The meeting ended with a vote of thanks to the Chair.

Secretary, Board of Academics

19.12.17

Chairman, Board of Academics

Annexure - 'A'

M. Tech. in Electrical Engineering (VLSI)

Specialization: Very Large Scale Integration (VLSI)

Duration: 4 semesters

Eligibility: Candidates with engineering field of studies such as BE or B. Tech in Electrical Engineering, Electronics & Communications, Instrumentation, Associate membership of professional bodies equivalent to B.Tech. (EEE/EE/ECE/IN) and M.Sc. in Electronics Science are eligible for this course. (As per ordinance and regulations for M.Tech./M.Sc. of IIT Mandi)

Selection: The candidates are selected through an All India entrance examination (GATE) followed by an interview. Total number of students will be **12**. The sponsored and government organization will be exempted from GATE examination. However, other eligible conditions are made as such for sponsored candidates. (As per ordinance and regulations for M.Tech./M.Sc. of IIT Mandi)

Objectives of the program:

After undergoing this program, the students will acquire both theoretical knowledge and practical skills in Electrical Engineering with specialization of VLSI and chip designing. The first semester of the course curriculum focuses on the Electrical Engineering core courses which can be supported to learn advance courses of VLSI specialization in preceding semesters. During M. Tech. theses, the students will use VLSI design, testing and fabrication laboratories. For a better insight of the specialization, the core laboratories for VLSI design and fabrication have been designed with considering experimental understanding of the Specialization Core courses. The laboratory experiments will build the basic concepts and the advanced concepts for chip designing. The VLSI laboratories will be the part of VLSI center of IIT Mandi. Moreover, these VLSI laboratories will be further useful for undergraduate students of IIT Mandi, in advance learning of B. Tech. with VLSI as minor area. The UG students will also use the VLSI center facility to execute their major technical project. It is envisaged that adjunct faculty from industry such as SCL (Mohali), STMicroelectronics, Texas instruments, Analog Devices, NXP, Synopsis, Cadence, Mentor Graphics etc. will be engaged to provide industrial experiences to M. Tech students.

The proposed M. Tech. course is with the vision of upcoming center for design and fabrication of electron devices (C4DFED) at IIT Mandi. The proposal is also a part of the special man-power development project from system to chip design (SMDP-C2SD) under the Department of Electronics and Information Technology (DeitY). The DeitY will be funding for the designed chip as a part of the M. Tech. theses under the India Chip Program (CDAC Noida). This initiative to fulfil the goal of development of country in the vision and mission of make India.

Conversion of M.Tech. to Ph.D. Program

There is a provision for meritorious students to convert from M.Tech. to Ph.D program. The criteria and terms and conditions will be formulated by the concerned school and must be approved by the Senate.

How is this program different?

- Very strong industry oriented curriculum
- Experiments/practical based learning,
- Industry oriented courses,
- The chip designing tools (Cadence, Mentor Graphics, Sylvaco, Centaurus, Comsol) based learning. These tools are the latest one and used in all the VLSI industries.
- 100 Class and 1000 class clean room facility available at IIT Mandi for device fabrications.
- Sophisticated instrumentations facility available for device fabrications and characterizations
- Learning design as well as fabrication aspects of the chip,
- Generate and trained manpower for semiconductor design and upcoming fab-line in India.
- There is a vast market opportunities for the graduating students.

Faculty strength for teaching courses:

<u>Core VLSI specilized faculties who can teach as well as guide the M. Tech. students</u>

1. Dr. Hitesh Shrimali (SCEE): Analog and mixed signal VLSI design (circuit designing)
2. Dr. Satinder Kumar Sharma (SCEE): VLSI Technology, Semiconductor device physics, MEMS/NEMS and memory design
3. Dr. Shubhajit Roy Chowdhury (SCEE): Embedded system, FPGA, EDA, VHDL and system level design
4. Dr. Viswanathan Balakrishnan (SE): Nano manufacturing and Nano materials
5. Dr. Kunal Ghosh (SCEE): Microelectronics and solar and photovoltaic devices

<u>Faxculty for computer organization and architecture</u>

1. Dr. Dileep A. D. (SCEE): Computer organization and architectures, VHDL, and system level programming

Course Structure:

- ***The first year is devoted to the course work.***
- ***The second year is devoted to the advance courses and project work.***

Curriculum Structure:

Sr. No.	*Curriculum Structure Detail*	*Credits*
1.	Electrical Engineering Cores	**12**
2.	VLSI Specialization Cores	**11**
3.	VLSI Specialization Electives	**13**
4.	Electives outside specialization	**6**
	Technical Communication	**1**
5.	M. Tech. dissertation	**28**
6.	**Total No. of Credits**	**71**

Semester wise distribution:

Semester-I	**18**
Semester-II	**19**
Semester-III	**16**
Semester-IV	**18**

Course Structure:

FIRST SEMESTER (1st Sem)

Course No.	Title of the course	L-T-P-C	Credits	Lab/space/tools requirement status	Remarks
EE 512	CMOS Analog IC design	3-0-2-4	4	VLSI design lab is allotted in Mandi. The simulation tools will be available before program starts, from SMDP project.	Specialization Core-1
EE XXXP	CMOS Digital IC design Laboratory	0-0-3-2	2	Digital testing laboratory space is needed. The list of required equipments are at the end.	Specialization Core Lab-1
EE XXX	Microelectronic devices and modeling	3-0-0-3	3	Fabrication lab Space is available in Mandi. Laboratory is functional with required equipments are available in IIT Mandi academic block.	Electrical Engineering Core
CS XXX	Advance Digital Signal Processing	3-0-0-3	3		Electrical Engineering core
CS 507	Advance Computer Architectures	3-0-0-3	3		Electrical Engineering core
MA XXX	Numerical Methods for Engineers	3-0-0-3	3		Electrical Engineering core
	Total		**18**		

SECOND SEMESTER (2nd Sem)

Course No.	Title of the course	L-T-P-C	Credits	Lab/space/tools requirement status	Remarks
EE 611	VLSI technology	3-0-0-3	3	Laboratory is functional with required equipments are available in IIT Mandi academic block.	Specialization core-1
EE XXXP	VLSI fabrication Laboratory	0-0-3-2	2	Laboratory is functional with required equipments are available in IIT Mandi academic block.	Specialization Lab-2
EEXXX	Elective-I	3-0-2-4	**4**		Specialization Elective (VLSI System Design)
EE XXX	Elective - II	3-0-0-3	3		Specialization Elective (VLSI Technology)
HS XXX	Elective - III	3-0-0-3	3		Free elective
YY XXX	Elective - IV	3-0-0-3	3		Free elective
YY XXX	Technical Communication*	1-0-0-1	1		
	Total		**19**		

In second semester, Electives-I & II (Design/Fabrication) will be offered with the help of industry .experts.

Elective –I

- EE 619 - Mixed signal VLSI Design **(3-0-2-4)**
- EE XXX - Embedded system Design **(3-0-2-4)**
- EE XXX - Biomedical systems **(3-0-2-4)**
- EE XXX - Mathematical Modeling for Signal Processing **(3-0-2-4)**

Elective –II

- EE XXX - Fundaments of photonic devices **(3-0-0-3)**
- EE XXX - Organic electronics **(3-0-0-3)**
- ME XXX - Nanomanufacturing **(3-0-0-3)**
- EE XXX - Sensors and transducers **(3-0-0-3)**
- EM XXX - Photovoltaics **(3-0-0-3)**
- Available course from TU9, Denmark university or NUS faculty.

Elective-III and Elective-IV (Free Elective from SHSS, SBS and SE) – (3-0-0-3)

The students can choose any elective from the school of humanities and social sciences (SHSS), the school of basic science (SBS) and the school of engineering (SE) for Elective-III.

THIRD SEMESTER (3rd Sem)

Course No.	Title of the course	L-T-P-C	Credits
EE XXX	Elective V:	3-0-0-3	3
EE XXX	Elective VI:	3-0-0-3	3
EE XXX	Master of Technology Dissertation – part - I	0-0-20-10	10
	Total		**16**

Elective –V

- EE XXX - Advanced embedded system **(3-0-0-3)**
- EE XXX - CAD for VLSI Design **(3-0-0-3)**
- EE XXX - Optical Devices and high Speed Communication **(3-0-0-3)**
- EE XXX - VLSI Test and Verification **(3-0-0-3)**

Elective –VI

- EE XXX - Nano electronics and Microfabrication **(3-0-0-3)**
- EE XXX ± MEMS/NEMS **(3-0-0-3)**
- EE XXX - Advance optoelectronics devices **(3-0-0-3)**
- EE XXX - Organic electronics **(3-0-0-3)**
- EE XXX - Sensors and transducers **(3-0-0-3)**

FOURTH SEMESTER (4th Sem)

Course No.	Title of the course	L-T-P-C	Credits
EEXXX	Master of Technology Dissertation – part - II	3-0-0-3	18
	Total		**18**

Syllabus

- **Electrical Engineering core courses**

- **EEXXX - Microelectronic devices and modeling** (3-0-0-3)

The objective of the course is to provide the knowledge for understanding concepts of semiconductor devices. The first part of the course provides an introduction to the basic physics of electrons in solids, quantum mechanics, and solid-state physics needed to understand nano-electronic devices. The second part is devoted to the fundamental theory of electron dynamics, carrier transport including ballistic transport, drift, diffusion, and recombination/generation. The third part of the course applies the fundamentals to describe the operation of several basic semiconductor devices: p-n junctions, metal-semiconductor junctions, Diodes, metal oxide semiconductor field effect transistors (MOSFETs), Complementary MOSFETs (CMOS) and Bipolar Junction Transistors (BJTs). The course will also cover topics which will be useful for the compact modeling of semiconductor devices.

- **EEXXX - Digital Signal Processing** (4-0-0-4)

Digital Signal Processing Introduction, Digital Systems, Characterization Description, Testing of Digital Systems, LTI Systems Step & Impulse Responses, Convolution, Inverse Systems,Stability,FIR & IIR, FIR & IIR; Recursive & Non Recursive, Discrete Time Fourier Transform, Discrete Fourier Transform (DFT), Introduction to Z Transform, Z Transform, Discrete Time Systems in the Frequency Domain, Simple Digital Filters, All Pass Filters, Complex Filters, Linear Phase filters, Complementary Transfer Function, Compensatory Transfer Functions, Test for Stability using All Pass Functions, Digital Processing of Continuous Time Signals, Problem Solving Session: FT, DFT,& Z Transforms, Analog Filter Design, Analog Chebyshev LPF Design, Analog Filter Design (Contd.): Transformations, Analog frequency Transformation, Digital Filter Structures, IIR Realizations, All Pass Realizations, Lattice Synthesis, FIR Lattice Synthesis, FIR Lattice (Contd.) and Digital Filter Design, IIR Filter Design, IIR Design by Bilinear Transformation, Digital to Digital Frequency Transformation, FIR Design, FIR Digital Filter Design by Windowing, FIR Design by Windowing & Frequency Sampling, Solving Problems on DSP Structures, FIR Design by Frequency Sampling, FIR Design by Frequency Sampling.

- **CS507 - Advance Computer Architectures** (3-0-0-3)

Processors Classification & Architectural Design Dimensions including Applications, Technology, Power and Performance Requirements, Instruction Set Architecture : CISC and RISC, Data Parallelism: Data and Controlled Dependencies and methods to manage these dependencies, Instruction Level Parallelism : Pipelined Implementation without and with multiple functional units, Static and Dynamic scheduling, Branch Prediction strategies, OpenCL OR Cuda Programming, Thread Parallelism, GPU & Multi-core Architecture, Bus Architecture, Memory Hierarchy with focus on Cache design, Heterogeneous Processing Units (HPU), Example Processors.

- **MAXXX - Numerical Methods for engineers** (3-0-0-3)

The goal of the course is to teach students how to apply computational methodologies to solve engineering problems when no closed-form, analytical solution exists. Achievement of this goal requires learning the basics of structured programming as well as learning how to combine engineering knowledge, judgment, and intuition to develop reasonable approximations through the engineering modeling process. Emphasis will be placed on understanding the basic concepts behind the various numerical methods studied, implementing basic numerical methods using the MATLAB structured programming environment, and utilizing more sophisticated numerical methods provided as built-in MATLAB functions.

VLSI core courses

- **EE 512 - CMOS Analog IC design (3-0-2-4) and EE XXXP - CMOS digital IC design laboratory (0-0-3-2)**

This course will teach the fundamentals and advance design techniques of CMOS analog circuits for the mixed-signal VLSI applications such as ADC, DAC, PLL and analog memory design. The topics include process background, current mirrors, differential amplifiers, noise associated with circuits, frequency response, stability, different feedback topology and the design of operational amplifier.

The laboratory course will also cover the analysis and the design of CMOS digital integrated circuits considering the applications such as memories (DRAM, SRAM, DDR), processor design. The experiments include models of wires, capacitive coupling, inverter design, the design of combinational gates, sequential circuits using CMOS technology. The objective will cover the concept of the understanding of signal integrity. The course deals will extensive use of Cadence Spectre, MentorGraphics Eldo for the schematic, the simulations and the layout design including parasitic extracted capacitors and inductors at various frequencies.

- **EE 611 - VLSI Technology (3-0-0-3), and EEXXXP - fabrication laboratory (0-0-3-2)**

VLSI Technology course designed to build up the in depth understanding among the B.Tech students and MS Ph.D scholars about the VLSI state of art Technology. This course consists the class lectures based on advanced device fabrication technology which also includes the hands-on assignments of future device structures in the Nanoelectronics and VLSI Technology Lab. The major goal of this course is to make the students familiarized with device fabrications and demonstrate the basic concepts of device fabrications such as Clean room, Vacuum technology, thin films deposition by physically and chemically etc. Additionally, to illustrate the students the concepts discussed in the class room teaching and to give an opportunity to build, feel and test real systems in the lab. In addition to this, class room discussion with regard to advanced lithography, MOS, MOSFET, CMOS device fabrication and characterization also included. Moreover, the application orientated devices such as MEMS, Bio sensors will also be fabricated by the students and scholar in the nanoelectronics and VLSI technology lab. As summarized, the objective of this course is to provide an understanding of microelectronics fabrication processing technologies.

VLSI Elective courses

- **EE 619 - Mixed signal VLSI Design (3-0-0-3)**

Analog and discrete-time signal processing, Analog integrated continuous-time and discrete-time (switched-capacitor) filters, basics of analog-to-digital converters (ADC), basics of digital-to-analog converters (DAC), successive approximation ADCs., dual slope ADCs, high-speed ADCs (e.g. flash ADC, pipeline ADC and related architectures), high-resolution ADCs (e.g. delta-sigma converters), mixed-Signal layout, interconnects, phase locked loops, delay locked loops. The course deals will extensive use of Cadence Spectre, MentorGraphics Eldo for the schematic, the simulations and the layout design including parasitic extracted capacitors and inductors at various frequencies.

- **EE XXX - Embedded system Design (3-0-0-3)**

Introduction to embedded computing, RISC architecture, S/W, Development environment, cross compiler, linker, debugger, stand alone system , ARM architecture, and ARM/THUMB instruction set, DSP, memories, clock and power management. Topics will range from current issues in nanoscale CMOS, to new device concepts that take the advantage of quantum mechanical phenomena that emerge on the nanometer scale, including the discreteness of electron charges. Another focus in nanoelectronics research is the advancement of nanofabrication technology that enables the creation of nanostructures with ever decreasing feature dimensions.

- **EE XXX - Biomedical systems (3-0-0-3)**

Introduction to Biomedical Systems, Anatomy and Physiology Biomedical sensing, Bio-signal processing, Biomedical embedded systems, Moral and ethical issues in developing Biomedical Systems, Course Project.

- **EE XXX - Mathematical Modeling for Signal Processing (3-0-0-3)**

In the field of signal processing we encounter problems which requires mathematical rigor – mostly in the area of linear algebra, functional analysis, optimization and estimation theory. This course develops the mathematical framework required for signal processing which consists of certain mathematical tools as well as algorithms. How these mathematical concepts are reflected in signal processing is brought out. After finishing this course the students will be in a better position to read and appreciate the current literature and problems in this area.

Course will cover Linear algebra and representation in vector spaces, Linear operator theory and matrix factorization, Estimation theory, Non-linear programming/optimization.

- **EE XXX - CAD for VLSI design (3-0-0-3)**

The course focuses on a general introduction to VLSI design flow and CAD tools algorithms and VLSI physical design (layout). It covers soft cells, hard cells, partitioning, placement, floorplanning, routing (global and detailed), and compaction. The course will also discuss why and how to partition a design process into macro-model problems and will study how to design good algorithms to solve each of those micro-model problems.

- **EE XXX - Fundamentals of photonic devices (3-0-0-3)**

Duality of light, Interaction light matter, Physics of semiconductor devices, Use of semiconductor lasers for telecommunications, Semiconductor material, Overview of active materials bulk, quantum well, wire dot and quatum dot. description of photonics band-gap materials.

- **EE XXX - Organic electronics (3-0-0-3)**

Synthesis of Organic Semiconductors, Charge Generation and Transport and Optoelectronic Characterization of Organic Semiconductors, Device Application of Organic Semiconductors. Explain how organic electronic devices operate and how to apply known equations to evaluate device performance, Critique the potential for organic electronic materials to supplement or replace inorganic semiconducting devices.

- **ME XXX – Nanomanufacturing (3-0-0-3)**

Nanomanufacturing involves large scale, reliable, economic and controlled production of nano scale materials, structures, devices and products. This course will cover various aspects of nanomanufacturing with major emphasis on the growth of 1D (CNT, Si nanowire) and 2D nanostructures (Graphene and other 2D materials) from chemical vapor deposition, thin film deposition techniques, self-assembly, nanopatterning along with several lithography and microfabrication techniques. This course also will include techniques involved in nanoscale characterization and fabrication.

- **EE XXX - Sensors and transducers (3-0-0-3)**

The terminology used for characterizing the performance of sensors. Discussion of the physical phenomena and devices which can be used for measuring displacement, velocity, acceleration, force, pressure, flow, strain, temperature, radiation and concentrations of chemical species. Identification of sources of uncertainty in measurements, use of simulated data for error analysis, techniques for improving the signal-to-noise ratio.

- **EM XXX – Photovoltaics (3-0-0-3)**

The objective of the course is to develop an understanding of the necessary ideas of photovoltaic sciences. The course is broadly divided into three modules, with each separately covering the topics of photovoltaic devices, PV systems and PV technology. On the completion of the course, the students will have a good understanding of the functioning of solar cells, along with requisite knowledge of PV systems and available photovoltaic technologies.

- **EE XXX - Optical Devices and high Speed Communication (3-0-0-3)**

Overview of optical properties of semiconductors. The fundamental principles for understanding and applying optical fiber technology, fundamental behaviour of the individual optical components and their interactions with other devices. Lasers, LED's, optical fibers, light detectors, optical switches. Concepts and components of WDM and DWDM. A comprehensive treatment of the underlying physics such as noise and distortion in optical communications, light polarization, modulation and attenuation.

- **EE XXX - VLSI Test and Verification (3-0-0-3)**

Digital VLSI Design flow comprises three basic phases: Design, Verification and Test. The web course would cover theoretical, implementation and CAD tools pertaining to these three phases. Although there can be individual full courses for each of these phases, the present course aims at covering the important problems/algorithms/tools so that students get a comprehensive idea of the whole digital VLSI design flow. VLSI Design: High level Synthesis, Verilog RTL Design, Combinational and Sequential Synthesis Logic Synthesis (for large circuits). Verification Techniques: Introduction to Hardware Verification and methodologies, Binary Decision Diagrams(BDDs) and algorithms over BDDs. Combinational equivalence checking, Temporal

Logics, Modeling sequential systems and model checking, Symbolic model checking. VLSI Testing: Introduction, Fault models, Fault Simulation, Test generation for combinational circuits, Test generation algorithms for sequential circuits and Built in Self test.

- **EE 615 - Nano electronics and Microfabrication (3-0-0-3)**

Tunnel junction and applications of tunneling, Tunneling Through a Potential Barrier, Metal—Insulator, Metal-Semiconductor, and Metal-Insulator-Metal Junctions, Coulomb Blockade, Tunnel Junctions, Tunnel Junction Excited by a Current Source. Spintronics and Foundations of nano-photonics, Field Emission, Gate—Oxide Tunneling and Hot Electron Effects in nano MOSFETs, Theory of Scanning Tunneling Microscope, Double Barrier Tunneling and the Resonant Tunneling Diode, Introduction to lithography- Contact, proximity printing and Projection Printing, Resolution Enhancement techniques, overlay-accuracies, Mask-Error enhancement factor (MEEF), Positive and negative photo resists, Electron Lithography, Projection Printing, Direct writing, Electron resists. Lithography based on Surface Instabilities: Wetting, De-wetting, Adhesion, Limitations, Resolution and Achievable / line widths etc. Lift off process, Bulk Micro machining, Introduction to MEMS and NEMS, working principles, as micro sensors (acoustic wave sensor, biomedical and biosensor, chemical sensor, optical sensor, capacitive sensor, pressure sensor and thermal sensor), micro actuation (thermal actuation, piezoelectric actuation and electrostatic actuation–micro gripers, motors, valves, pumps, accelerometers, fluidics and capillary electrophoresis, active and passive micro fluidic devices, Pizoresistivity,Pizoelectricity and thermo electricity, MEMS/NEMS design, processing, Oxidation, Sputter deposition, Evaporation, Chemical vapor deposition etc. , Introduction – Scaling of physical systems – Geometric scaling & Electrical system scaling. The Single-Electron Transistor: The Single- Electron Transistor Single-Electron Transistor Logic, Other SET and FET Structures, Carbon Nanotube Transistors (FETs and SETs), Semiconductor Nanowire FETs and SETs,Coulomb Blockade in a Nanocapacitor, Molecular SETs and Molecular Electronics.

- **EE XXX – MEMS/NEMS (3-0-0-3)**

Introduction to MEMS and NEMS:MEMS and NEMS – multidisciplinary nature of MEMS/NEMS as micro sensors (acoustic wave sensor, biomedical and biosensor, chemical sensor, optical sensor, capacitive sensor, pressure sensor and thermal sensor), micro actuation (thermal actuation, piezoelectric actuation and electrostatic actuation,active and passive micro fluidic devices. Materials for MEMS/NEMS Silicon – Compatible material systems, Silicon, Silicon oxide and nitride, Thin metal films, Polymers, Other materials and substrates, Glass and fused quartz substrates, Important material properties and physical effects, Pizoresistivity, Pizoelectricity and thermoelectricity, Inter atomic bonds, Lithography, Lift off process, Bulk Micro machining, Etching Silicon fusion bonding, Anodic bonding, Silicon direct bonding, sol gel deposition methods, Self assembled mono layers, EFAB. LIGA electromagnetic micro drive, DRIEThermal management, Hermetic packaging, Electrical//Micro fluidic/and optical interconnects, Quality control-reliability and failure modes and analysis, Signal mapping transduction. MEMS/NEMS applications: Applications in automotive industry, health care, aerospace – industrial product consumer products – lab on chip – molecular machines – data storage devices – micro reactor – telecommunications, Servo systems.

Annexure ± I

Infrastructural support needed:

1. **Space required:** A 20'X20' space needed.
2. **Servers:** No. 3 for EDA tools installations
3. **Work Station:** No. 15
4. **Furniture needed:** 20 electrical lab workbenches are needed for VLSI design and testing laboratories.

Estimated Budget Requirement:

Phase – 1

	Item	Nos.	Total Price (in INR)
1	Servers	2	4,00,000/-
2	Computers	15	7,50,000/-
3	Arbitrary waveform generators	10	5,00,000
4	Mixed mode Oscilloscope	1	10,00,000
5	Spectrum analyzer	1	10,00,000
6	Logic probes	10	30,000
7	ARM Cortex M3 LPC1768 boards	10	5,00,000
8	ARM 920T board	5	3,00,000
9	LCD matrix keyboard interface kit	10	50,000
10	General Purpose I/O board	10	50,000
11	RFID module	10	50,000
12	GSM module	10	50,000
13	NI Elvis board	5	6,50,000
14	Variable power supply	10	1,00,000
15	Thin film resistivity measurement	1	20,00,000
	Total (first phase)		**Rs. 74,30,000/-**

Phase – 2

	Item	Nos.	Total Price (in INR)
1	E-Beam Evaporation	1	15,00,000/-
2	Thin film consumables	-	8,00,000/-
3	Lithography consumables	-	5,00,000/-
4	Silicon wafers	-	4,00,000/-
5	Dicing cutter machine	1	20,00,000/-
6	Ball Wire bonder	1	15,00,000/-
7	Microfluidic kit	1	10,00,000/-
8	Plasma cleaner	1	20,00,000/-
9	Lab wearers and chemicals (consumables)	-	5,00,000/-
	Total (second phase)		**Rs. 1,02,00,000/-**

Course structure:

- **The first year is devoted to the course work.**
- **The second year is devoted to the advance courses and project work.**

Curriculum Structure:		
Sr no	Curriculum structure detail	Credits
1	Electrical Engineering Cores	13 (earlier 12)
2	VLSI Specialization Cores	11
3	VLSI Specialization Electives	12-13 (earlier 13)
4	Electives outside specialization	6
5	Technical Communication	1
6	M. Tech. dissertation	28
7	Total No. of Credits	71-72 (earlier 71)

Semester wise distribution:	
Semester I	18
Semester II	19
Semester III	16
Semester IV	18

Course Structure:

FIRST SEMESTER (1st Sem)					
CourseNo.	**Title of thecourse**	**L-T-P-C**	**Credits**	**Lab/space/tools requirementstatus**	**Remarks**
EE 512	CMOS Analog IC design	3-0-2-4	4	VLSI design lab is allotted in Mandi. The simulation tools will be available before program starts, from SMDP project.	Specialization Core-1
EE 519P	CMOS Digital IC design Laboratory	0-0-3-2	2	Digital testing laboratory space is needed. The list of required equipments are at the end.	Specialization Core Lab-1
EE 520	Microelectronic devices and modeling	3-0-0-3	3	Fabrication lab Space is available in Mandi. Laboratory is functional with required equipments are available in IIT Mandi academic block.	Electrical Engineering Core
EE620	Advance Digital Signal Processing	3-0-0-3	3		Electrical Engineering core
EE529	Embedded system	3-0-2-4	4		Electrical Engineering core
ME 504	Numerical Methods for Engineering Computations	3-0-0-3	3		Electrical Engineering core
	Total		**18**		

SECOND SEMESTER (2nd Sem)					
CourseNo.	**Title of thecourse**	**L-T-P-C**	**Credits**	**Lab/space/tools requirementstatus**	**Remarks**
EE 611	VLSI Technology	3-0-0-3	3	Laboratory is functional with required equipments are available in IIT Mandi academic block.	Specialization Core-1
EE 611P	VLSI Fabrication Laboratory	0-0-3-2	2	Laboratory is functional with required equipments are available in IIT Mandi academic block.	Specialization Lab-2
EEXXX	Elective-I	3-0-2-4	4		Specialization Elective (VLSI System Design)
EE XXX	Elective -II	3-0-0-3	3		Specialization Elective (VLSI Technology)
HSXXX	Elective-III	3-0-0-3	3		Free Elective
YY XXX	Elective-IV	3-0-0-3	3		Free Elective
YY XXX	Technical Communication	1-0-0-1	1		
	Total		**19**		

In second semester, Electives-I & II (Design/Fabrication) will be offered with the help of industry experts.

Elective –I

- EE 619 Mixed signal VLSI Design **(3-0-2-4)**
- CS 507 Advanced Computer Architectures **(3-0-0-3)**
- EE XXX Biomedical systems **(3-0-2-4)**
- EE XXX Mathematical Modeling for Signal Processing **(3-0-2-4)**

Elective –II

- EE XXX Fundaments of photonic devices **(3-0-0-3)**
- EE XXX Organic electronics **(3-0-0-3)**
- ME XXX Nanomanufacturing **(3-0-0-3)**
- EE XXX Sensors and transducers **(3-0-0-3)**
- EM XXX Photovoltaics **(3-0-0-3)**
- Available course from TU9, Denmark university or NUS faculty.

• Elective-III and Elective-IV (Free Elective from SHSS, SBS and SE) – (3-0-0-3)

The students can choose any elective from the school of humanities and social sciences (SHSS), the school of basic science (SBS) and the school of engineering (SE) for Elective-III.

THIRD SEMESTER (3rd Sem)

Course No.	Title of the course	L-T-P-C	Credits
EE XXX	Elective V:	3-0-0-3	3
EE XXX	Elective VI:	3-0-0-3	3
EE XXX	Master of Technology Dissertation – part - I	0-0-20-10	10
	Total		**16**

Elective –V

- EE XXX - Advanced embedded system **(3-0-0-3)**
- EE XXX - CAD for VLSI Design **(3-0-0-3)**
- EE XXX - Optical Devices and high Speed Communication **(3-0-0-3)**
- EE XXX - VLSI Test and Verification **(3-0-0-3)**

Elective –VI

- EE XXX - Nano electronics and Micro fabrication**(3-0-0-3)**
- EE XXX – MEMS/NEMS **(3-0-0-3)**
- EE XXX - Advance optoelectronics devices **(3-0-0-3)**
- EE XXX - Organic electronics **(3-0-0-3)**
- EE XXX - Sensors and transducers **(3-0-0-3)**

FOURTH SEMESTER (4^{th} Sem)

Course No.	Title of the course	L-T-P-C	Credits
EEXXX	Master of Technology Dissertation – part - II	3-0-0-3	18
	Total		**18**

IIT Mandi
Proposal for a New Course

Course Number	: EE529
Course Name	: Embedded Systems
Credits	: 3-0-2-4.
Pre-requisite	: IC161 - Applied Electronics, CS201 – Computer Organization or any course on microprocessors or Equivalent
Intended for	: BTech Computer Science Engineering (CSE) and Electrical Engineering (EE), MS, M. Tech. & PhD.
Distribution	: Elective for Third and Final year B. Tech (CSE/EE), MS, M. Tech. in VLSI/Signal Processing and Communication/Power Electronics and Drives & PhD
Semester	: Even or Odd.

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1. Preamble:

The Embedded Systems course aim at building up an in depth understanding among the advanced B.Tech / M.Tech / M.S./ Ph.D students of embedded systems architecture, design space exploration and design optimization of embedded systems through a perfect synergy of class lectures and hands on assignments. The goal is to illustrate the concepts discussed in the classroom teaching and to give students an opportunity to build, feel and test real systems. Since the embedded systems of today are centered around a wide variety of embedded cores such as micro-controllers and FPGA, topics in lecture should focus around the system design issues with the different types of embedded cores. Finally, topics of recent interest such as hardware software co-design, Internet of Things give the student an idea of the state of the art technological practices in Embedded Systems.

2. Course Modules with Quantitative Lecture Hours:

1. **Introduction to embedded systems:** Understanding an embedded system, design metrics, design challenges, technologies for embedded systems. **(2 Lectures)**

2. **Custom Single Purpose Processor for Embedded Systems**: Design of data-paths and controllers, finite state machines, custom single purpose processor design at RT level, optimizing custom single purpose processors. **(3 Lectures)**

3. **Hardware Description Language:** Introduction to hardware description language, overview of structural, behavioral and dataflow modeling of digital systems using hardware description language, notion of finite state machines, delay modeling, memory modeling, synthesizable & non-synthesizable HDL codes for digital system design. **(3 Lectures)**

4. **Introduction to FPGA:** Introduction to complex digital systems design, notion of programmable logic devices, overview of FPGA architecture, realization of data-path and controller, timing analysis of data-path and controller, synthesis, placement, routing, performance optimization. **(3 Lectures)**

5. **FPGA based systems design:** Implementation of simple systems using FPGA exercising the timing closure paths. **(2 Lectures)**

6. **Physical design automation of embedded systems (from the perspective of custom single purpose processors for embedded systems):** Partitioning, floor-planning, placement, routing; clock design considerations, timing margins, clock skew, clock distribution networks. **(3 Lectures)**

7. **Dynamically reconfigurable Embedded Systems:** Static versus dynamic reconfiguration of embedded systems, full versus partial reconfiguration, voltage scaling and power management issues in dynamic reconfiguration. **(3 Lectures)**

8. **Introduction to Microcontrollers:** Introduction to microcontrollers, overview of architecture of a typical microcontroller such as AVR microcontroller, addressing, assembly language programming. **(4 Lectures)**

9. **Memory interfacing:** Memory technologies – SRAM, DRAM and ROM, different types of DRAM architectures – 2D RAM, FPMDRAM, EDODRAM, SDRAM, RDRAM, DDRRAM, DDR2RAM, etc, different types of ROM- PROM, EPROM, EEPROM, memory interfacing circuits, single cycle versus multiple cycle interfacing, timing diagrams, etc. **(3 Lectures)**

10. **Interfacing with I/O devices:** Port and bus based I/O, Memory mapped and I/O mapped I/O, register and tristate buffer based I/O interfacing, arbitration methods – priority, daisy chain and network oriented arbitration methods, serial protocols – SPI and I2C. **(4 Lectures)**

11. **Timers and Counters:** Timer/counter programming, notion of watch dog timers and real time clocks. **(2 Lectures)**

12. **Interrupt processing:** Introduction to interrupts, external versus internal interrupts, software versus hardware interrupts, synchronous versus asynchronous interrupts, single interrupt versus multiple interrupt systems, prioritization of interrupts, inversion of interrupt priorities, inheritance of interrupt priorities and associated protocols.**(4 Lectures)**

13. **Real world interfacing of microcontrollers:** Interfacing with simple devices such as LCD, keyboard, motor control, sensors, LED 7 segment display, DTMF decoder, etc. **(2 Lectures)**

14. **Hardware Software Codesign:** Notion of hardware software partitioning, graph based and pareto optimal approaches to hardware software partitioning, resource and timing constrained hardware software partitioning. **(3 Lectures)**

15. **Internet of Things (IoT):** Overview of Internet of Things, IoT architecture, Communication protocols, Notion of internet of everything. **(1 Lecture)**

Laboratory Experiments: Laboratory exercises based on timers and counters, interrupts, serial peripheral interface, inter-integrated circuit, hardware description language based hardware modeling of embedded cores, hybrid embedded processors, FPGA implementation of embedded processor architectures.

3. Text Books:

1. F. Vahid and T. Givargis, "Embedded Systems: A Unified Hardware Software Introduction", John Wiley and Sons, 2011.

4. References:

1. G. Nicholescu and P.J. Mosterman, "Model based design of Embedded Systems", CRC Press, 2009.
2. Dhananjay Gadre, "Programming and Customizing the AVR microcontroller", Tata McGraw Hill, 2014.
3. Wayne Wolf, "FPGA based Systems Design", Pearson Education, 2003.
4. Volnei A. Pedroni, "Circuit Design with VHDL", The MIT Press, 2004.
5. Steve Kilts, "Advanced FPGA Design: Architecture, Implementation and Optimization", J. Wiley and Sons, 2007.
6. Seetharaman Ramachandran, "Digital VLSI Systems Design", Springer Verlag, 2012.
7. Peter J. Ashenden, "The designer's guide top VHDL", Morgan Kaufmann, 2008.
8. Charles H. Roth Jr., "Digital Systems Design using VHDL", Cengage Learning, 2014.

5. Similarity Content Declaration with Existing Courses:

S.N.	Course Code	Similarity Content	Approx. % of Content
1.	EE208P	Hardware Description Languages, Introduction to FPGA, Introduction to Microcontrollers (Total 10L)	25%

6. Justification for new course proposal if cumulative similarity content is > 30%:N/A

Approvals:

Other Faculty interested in teaching this course: Dr. Rahul Shrestha, Dr. Srikant Srinivasan

Proposed by: Dr. Shubhajit Roy Chowdhury School: SCEE

Signature: ____________________ Date: ____________

Recommended/Not Recommended, with Comments:

____________________________________ Date: ____________
Chairman, CPC

Approved/Not Approved

____________________________________ Date: ____________
Chairman, Senate

Note:
The course has been discussed in CIG and modified as per their suggestion.